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APPLICATION NO.	F	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/764,208	(	01/19/2001	Jae-Choon Lee	0630-1210P	7426	
2292	7590	12/14/2001				
		KOLASCH & BI	EXAMINER			
PO BOX 74 FALLS CH	-	A 22040-0747	LEVI, DAMEON E			
				ART UNIT	PAPER NUMBER	
				2841		
				DATE MAILED: 12/14/2001	DATE MAILED: 12/14/2001	

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No. pplicant(s)						
<b>j</b>	Office Action Summary	09/764,208	HWANG ET AL.					
	Onice Action Summary	Examin r	Art Unit					
_	The MAILING DATE of this communication and	Dameon E Levi	2841					
Period fo	The MAILING DATE of this communication app or Reply	pears on the cover sheet with the c	orrespondence address					
THE   - External after - If the - If NC - Failu - Any	ORTENED STATUTORY PERIOD FOR REPLY MAILING DATE OF THIS COMMUNICATION. nsions of time may be available under the provisions of 37 CFR 1.1 SIX (6) MONTHS from the mailing date of this communication. It is period for reply specified above is less than thirty (30) days, a reply operiod for reply is specified above, the maximum statutory period or reto reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be timy within the statutory minimum of thirty (30) day; will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE.	nely filed s will be considered timely. the mailing date of this communication. D. (35 U.S.C. 6, 133)					
1)	Responsive to communication(s) filed on	·						
2a) <u></u> ☐	This action is <b>FINAL</b> . 2b)⊠ Th	is action is non-final.						
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Dispositi	on of Claims							
4)🖂	Claim(s) $\underline{1-4}$ is/are pending in the application.							
	4a) Of the above claim(s) is/are withdrawn from consideration.							
5)	5) Claim(s) is/are allowed.							
6)[	6) Claim(s) 1-4 is/are rejected.							
7)	Claim(s) is/are objected to.							
8)□	Claim(s) are subject to restriction and/or	r election requirement.						
Applicati	on Papers							
9) The specification is objected to by the Examiner.								
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.								
—	Applicant may not request that any objection to the	- · · · · · · · · · · · · · · · · · · ·	` '					
11) ☐ The proposed drawing correction filed on is: a) ☐ approved b) ☐ disapproved by the Examiner.								
If approved, corrected drawings are required in reply to this Office action.								
	The oath or declaration is objected to by the Exa	aminer.						
•	nder 35 U.S.C. §§ 119 and 120							
•	Acknowledgment is made of a claim for foreign	priority under 35 U.S.C. § 119(a)	-(d) or (f).					
a)[	☑ All b) Some * c) None of:							
	1. Certified copies of the priority documents							
	Certified copies of the priority documents		<del></del>					
	3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  See the attached detailed Office action for a list of the certified copies not received.							
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).								
a) The translation of the foreign language provisional application has been received.  15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.								
Attachment		, 1,						
2) 🔲 Notice	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal P	(PTO-413) Paper No(s) atent Application (PTO-152)					
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## **DETAILED ACTION**

## Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "power pin" in **claim 3** is used by the claim to mean " a power board," while the accepted meaning is " power pin." The language is ambiguous and mis-discriptive.

The claims are generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. The phrase, "thereby reducing the pins in number of the socket" in **claim 5** is an example of narration and indefiniteness.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki et al US Patent 5,295,044 in view of Umeda US Patent 5,398,160.



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Regarding claim 1, Araki et al discloses a semiconductor device comprising:

- a ceramic PCB and an epoxy PCB disposed inside a module body (see column 9, lines 38-42, elements 43, 44 Fig 6)
- a power element and signal elements respectively mounted on the upper portion of each PCB (see column 10, lines 20-22 and 28-30)
- a groove made at the lower side surface and the middle side surface of the module body (see element(s) 71 Fig<sup>2</sup>).
- The examiner notes that a socket placed between two PCBs for connection purposes is conventional in the art and is deemed only as an alternate means.

Araki et al does not disclose:

- a power pin for receiving a power signal from an external source mounted on the ceramic PCB;
- a signal pin for receiving various signals from an external source mounted on the epoxy PCB

Umeda discloses a pin arrangement as disclosed by the applicant (see elements 15 and 18, Fig. 4, column 1 lines 46-48 and lines 59-60)

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the power and signal pins upon the ceramic and epoxy PCBs respectively for the purpose of ensuring direct and reliable signal transmission and electrical conductivity between the respective



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circuits and the corresponding external devices or circuits to which they are connected.

**Regarding claim 2**, the examiner notes that aluminum wire bonding and gold wire bonding to mount elements on PCBs is conventional in the art because of the good electrical conductivity and high reliability properties of aluminum and gold.

**Regarding claim 3**, and, as best understood by the examiner, the mounting of power and signal pins to PCBs by the technique of soldering is conventional in the art.

**Regarding claim 4**, as best understood by the examiner, Araki et al discloses the instant claimed invention except;

- the power pin is mounted on the ceramic PCB;
- the signal pin is mounted on the epoxy PCB.

Umeda discloses a pin arrangement as disclosed by the applicant (see elements 15 and 18, Fig. 4, column 1 lines 46-48 and lines 59-60).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to mount the power and signal pins upon the ceramic and epoxy PCBs respectively for the purpose of ensuring direct and reliable signal transmission and electrical conductivity between the respective PCBs and the corresponding external devices or circuits to which they are connected.



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## Conclusion

 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Araki et al US Patent 5,295,044 discloses a semiconductor device.

Umeda US Patent 5,398,160 discloses a compact power module with a heat spreader

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dameon E Levi whose telephone number is (703) 305-0426. The examiner can normally be reached on Mon.-Fri. (9:00 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on (703) 308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0058.

Dameon E Levi Examiner Art Unit 2841

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December 5, 2001

JNRardh

Jayprakash N. Gandhi Primary Examiner Technology Center 2800